

LIST OF PRIOR ART CITED BY APPLICANT (PTO-1449)				ATTY. DOCKET NO. INTEL-0062		APPLN. SERIAL NO. New U.S. Patent Application 10/813169	
				APPLICANT(S) Peter HAZUCHA, Jianping XU, Gerhard SCHROM, Tanay KARNIK, Fabrice PAILLET, and Vivek K. DE			
				CUSTOMER NO. 34610			
				FILING DATE March 31, 2004		GROUP 2816 To be assigned	
U.S. PATENT DOCUMENTS							
EXAMINER'S INITIALS	*PATENT NO.	*ISSUE DATE	*INVENTOR NAME	CLASS	SUBCLASS	FILING DATE	
U.S. PATENT APPLICATION PUBLICATIONS							
	*PATENT APPLN. PUB. NO.	*PUB. DATE	*APPLICANT	CLASS	SUBCLASS		
U.S. PATENT APPLICATIONS							
	*APPLN. NO.	*FILING DATE	*INVENTOR	CLASS	SUBCLASS		
FOREIGN PATENT DOCUMENTS							
EXAMINER'S INITIALS	PATENT NO.	DATE	COUNTRY	CLASS	SUBCLASS	Translation Yes No	
OTHER ART (Including Author, Title, Date, Pertinent Pages, Publisher, Place of Publication, Etc.)							
DL	Patrik Larsson, "Resonance and Damping in CMOS Circuits with On-Chip Decoupling Capacitance;; IEEE Transactions on Circuits and Systems - I: Fundamental Theory and Applications, Vol. 45, No. 8, August 1998; pp. 849-858						
DL	Luca Amoroso et al., "Single Shot Transient Suppressor (SSTS) for High Current High Slew Rate Microprocessor;" 1999 IEEE; pp. 284-288						
DL	Michael Ang et al.; "WP 26.7 An On-Chip Voltage Regulator Using Switched Decoupling Capacitors" 2000 IEEE International Solid-State Circuits Conference; pp. 438-439						
EXAMINER	<i>Chadwick</i>			DATE CONSIDERED 4/17/05			

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.